UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,660	10/27/2003	Timothy Lance Blankenship	08211/0200250-US0/P05707	4239

38845 7590 04/04/2005

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

A1C

Office Action Summary	Application No.	Applicant(s)	
	10/694,660	BLANKENSHIP, TIMOTHY LANCE	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 7* is/are allowed.

6)☒ Claim(s) *1-5 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nebel (U. S. PAT. 6,392,440).

In claim 1, Nebel teaches all claimed features in Fig. 1, an input level translator circuit comprising: a first pass circuit (MP1) that is coupled to a full-range node (IN), to a first bias node (5), and to a high-range node (P1); a second pass circuit (MN1) that is coupled to the full-range node (IN), to a second bias node (6), and to a low-range node (N1); a first shunt circuit (MP21-MP22) that is coupled between the first bias node (5) and the high-range node (P1); and a second shunt circuit (MN21-MN22) that is coupled between the second bias node (6) and the low-range node (N1), wherein the second shunt circuit (MN21-MN22) includes a switch circuit (MN21) that is arranged to close (conducting) if a voltage (a voltage input into IN) associated with the full-range node corresponds to a logic high (logic 1).

In claim 2, Nebel teaches all claimed features in Fig. 1, an input level translator circuit comprising: a first pass circuit (MP1) that is coupled to a full-range node (IN), to a first bias node (5), and to a high-range node (P1); a second pass circuit (MN1) that is coupled to the full-range node (IN), to a second bias node (6), and to a low-range node (N1); a first shunt circuit (MP21-MP22) that is coupled between the first bias node (5)

and the high-range node (P1); and a second shunt circuit (MN21-MN22) that is coupled between the second bias node (6) and the low-range node (N1), wherein the first bias node (5) and the second bias node (6) have approximately the same voltage (2.5 Volts).

In claim 3, Nebel further teaches the input level translator circuit of claim 1, wherein the first shunt circuit (MP22) is configured to receive a first cascode bias voltage (LOW) at the first bias node (5), wherein the first cascode bias voltage is appropriate for biasing a cascode transistor (MP21).

In claim 4, Nebel further teaches the input level translator circuit of claim 1, wherein the first pass circuit (MP1) is configured to provide a high-range signal (5.0v) at the high-range node (P1) in response to a full-range signal (IN), the second pass circuit (MN1) is configured to provide a low-range signal (0v) at the low- range node (6) in response to the full-range signal, the full-range signal has a range from a low-voltage level (0v) to a high-voltage level (5.0v), the low-range signal has a range from the low-voltage level (0v) to an intermediate- voltage level (3.3v), the high-range signal has a range from the intermediate-voltage level (3.3v) to the high- voltage level (5.0v), and the intermediate voltage level is partway between the low-voltage level and the high-voltage level (0v<3.3v<5.0v).

In claim 5, Nebel further teaches the input level translator circuit of claim 1, wherein: the first bias node (5) is coupled to a gate of a p-type transistor (MP22) configured to operate as a cascode transistor (MP22), and the second bias node (6) is coupled to a gate of an n-type transistor (MN22) configured to operate as another cascode transistor (MN22).

In claim 8, Nebel further teaches the input level translator circuit of claim 1, wherein the first shunt circuit (MP21-MP22) is configured to influence a resistance between the first bias node (5) and the high-range node (P1) depending on a full-range signal (IN).

In claim 9, Nebel teaches all claimed features in Fig. 1, an input level translator circuit comprising: a first pass circuit (MP1) that is coupled to a full-range node (IN), to a first bias node (5), and to a high-range node (P1); a second pass circuit (MN1) that is coupled to the full-range node (IN), to a second bias node (6), and to a low-range node (N1); a first shunt circuit (MP21-MP22) that is coupled between the first bias node (5) and the high-range node (P1); and a second shunt circuit (MN21-MN22) that is coupled between the second bias node (6) and the low-range node (N1), wherein the first shunt circuit (MP21-MP22) is configured to isolate (disengage) the first bias node (5) from the high- range node (P1) if the full-range signal (IN) corresponds to a logic high (logic 1).

In claim 10, Nebel teaches all claimed features in Fig. 1, an input level translator circuit comprising: a first pass circuit (MP1) that is coupled to a full-range node (IN), to a first bias node (5), and to a high-range node (P1); a second pass circuit (MN1) that is coupled to the full-range node (IN), to a second bias node (6), and to a low-range node (N1); a first shunt circuit (MP21-MP22) that is coupled between the first bias node (5) and the high-range node (P1); and a second shunt circuit (MN21-MN22) that is coupled between the second bias node (6) and the low-range node (N1), wherein the first shunt circuit (MP21-MP22) is configured to short (connect or conduct) the first bias node (5)

from the high- range node (P1) if the full-range signal (IN) corresponds to a logic low (logic 0).

In claim 11, Nebel further teaches the input level translator circuit of claim 1, wherein the second shunt circuit (MN21-MN22) is configured to influence a resistance between the second bias node (6) and the low-range node (N1) depending on a full-range signal (IN).

In claim 12, Nebel further teaches the input level translator circuit of claim 1, wherein the first shunt circuit (MP21-MP22) is configured to short (connect) the high-range node (P1) to the first bias node (5) when a full-range signal (IN) corresponds to a first logic level (logic 0), and isolate (disconnect) the high-range node from the first bias node when the full-range signal corresponds to a second logic level (logic 1), and the second shunt (MN21-MN22) circuit is configured to short the low-range node (6) to the second bias node (N1) when a full-range signal (IN) corresponds to the second logic level (logic 1), and isolate the low-range node from the second bias node when the full-range signal corresponds to the second logic level (logic 0).

In claim 13, Nebel teaches all claimed features in Fig. 1, a method for translating a level for a full-range signal, comprising: converting the full-range signal (IN) into a high-range signal (3.6V when IN is at 5V; col.4, line 50) at a high-range node (N1); converting the full-range signal into a low-range signal (1.4V when IN is at 0 V; col. 5, line 1) at a low-range node (P1); and ensuring that at least one of: the low-range node (P1) is driven during a full cycle (two periods) of the full range signal, and the high-range node (N1) is driven during the full cycle of the full-range signal.

In claim 14, Nebel further teaches the input level translator circuit of claim 13, wherein the full-range signal (IN) has a range from a low-voltage level (0V) to a high-voltage level (5V), the low-range signal (1.4V) has a range from the low-voltage level (0V) to an intermediate-voltage level (2.5V), the high-range signal (3.6V) has a range from the intermediate-voltage level (2.5V) to the high-voltage level (5V), and the intermediate voltage level is partway (half of 5V) between the low-voltage level and the high-voltage level.

In claim 15, Nebel further teaches the input level translator circuit of claim 13, wherein ensuring that the high range node (N1) is driven comprises influencing (adjusting) a resistance between a first bias node (a node coupling gates of MN1 and MN22) and the high-range node (N1) depending on the full-range signal (IN is at 5V in this case); and ensuring that the low range node (P1) is driven comprises influencing (adjusting) a resistance between a second bias node (a node coupling gates MP1 and MP21) and the low-range node (P1) depending on the full-range signal (IN is at 0V in this case).

In claim 16, Nebel further teaches the input level translator circuit of claim 13, wherein ensuring that the high-range node (N1) is driven comprises shorting (connecting) the high-range node to the first bias node if the full-range signal corresponds to a first logic level (when IN is at 5V, MN1 closed); and ensuring that the low-range node (P1) is driven comprises shorting (connecting) the low-range node to the second bias node if the full-range voltage corresponds to the second logic level (when IN is at 0V, MP1 closed).

In claim 17, Nebel teaches all claimed features in Fig. 1, an input level translator circuit comprising: a first pass circuit (MP1) that is coupled to a full-range node (IN), to a first bias node (5), and to a high-range node (P1); a second pass circuit (MN1) that is coupled to the full-range node (IN), to a second bias node (6), and to a low-range node (N1); a first shunt circuit (MP21-MP22) that is coupled between the first bias node (5) and the high-range node (P1), wherein the first shunt circuit is configured to receive a p-type cascode bias signal (LOW) at the first bias node (5), wherein the first shunt circuit includes a switch circuit (MP21) that is arranged to close if a voltage associated with the full-range node corresponds to a logic low (IN is at 0V); and a second shunt circuit (MN21-MN22) that is coupled between a second bias node (6) and the low-range signal, wherein the second shunt circuit is configured to receive an n-type cascode bias signal (when IN is at 5V) at the second bias node.

In claim 18, Nebel further teaches the input level translator circuit of claim 17, wherein the full-range signal (IN) has a range from a low-voltage level (0V) to a high-voltage level (5V), the low-range signal (1.4V) has a range from the low-voltage level (0V) to an intermediate-voltage level (2.5V), the high-range signal (3.6V) has a range from the intermediate-voltage level (2.5V) to the high-voltage level (5V), and the intermediate voltage level is partway (half of 5V) between the low-voltage level and the high-voltage level.

In claim 19, Nebel further teaches the input level translator circuit of claim 17, wherein the first shunt circuit (MP21-MP22) is configured to short (connect) the high-range node (P1) to the first bias node (5) when a full-range signal (IN) corresponds to a

first logic level (logic 0), and isolate (disconnect) the high-range node from the first bias node when the full-range signal corresponds to a second logic level (logic 1), and the second shunt (MN21-MN22) circuit is configured to short the low-range node (6) to the second bias node (N1) when a full-range signal (IN) corresponds to the second logic level (logic 1), and isolate the low-range node from the second bias node when the full-range signal corresponds to the second logic level (logic 0).

Claim 20 corresponds to detailed circuitry already discussed similarly with regard to claim 13.

3. Claims 6 and 7 appear to comprise allowable subject matter.

Response to Arguments

4. Applicant's arguments filed 03/02/2005 have been fully considered but they are not persuasive.

Regarding claims 1 and 17, the Applicant argued that Nebel does not teach the second shunt circuit includes a switch circuit that is arranged to close if a voltage associated with the full-range node corresponds to a logic high; the Examiner respectfully disagrees because transistor MN21 is a switch circuit not diode MP11, as argued by the Applicant.

Regarding claim 2, The Examiner respectfully disagrees with the Applicant's augment that Nebel doest not teach the first bias node and the second bias node have approximately the same voltage because the first bias node (5) and the second bias node (6) have approximately the same voltage (2.5 Volts).

Regarding claims 13 and 20, the Examiner believes that Nebel inherently teaches the ensuring that at least one of: the low-range node is driven during a full cycle of the full range signal, and the high-range node is driven during the full cycle of the full-range signal because the structure of Nebel in Fig.1 is basically the same as the structure of the Applicant in Fig. 2; with the exception of the diodes MP11 and MN11. However, as pointed out in col. 4 lines 56-60, without the transistor MP11, leakage currents in the steady-state would charge the gate of transistor MN21 further, since the gate of a MOS transistors provides better insulation than a switch-off transistor. Since the circuit of Neble in Fig. 1 has the same electrical property of the Applicant's circuit in Fig. 2, Nebel teaches the ensuring that at least one of: the low-range node is driven during a full cycle of the full range signal, and the high-range node is driven during the full cycle of the full-range signal.

The rejection of claims 1-5 and 8-20 is maintained.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER